



# M74HC192

## SYNCHRONOUS UP/DOWN DECADE COUNTER

- HIGH SPEED :  
 $f_{MAX} = 55 \text{ MHz (TYP.) at } V_{CC} = 6V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4\text{mA (MIN)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:  
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE WITH  
 74 SERIES 192



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC192B1R	
SOP	M74HC192M1R	M74HC192RM13TR
TSSOP		M74HC192TTR

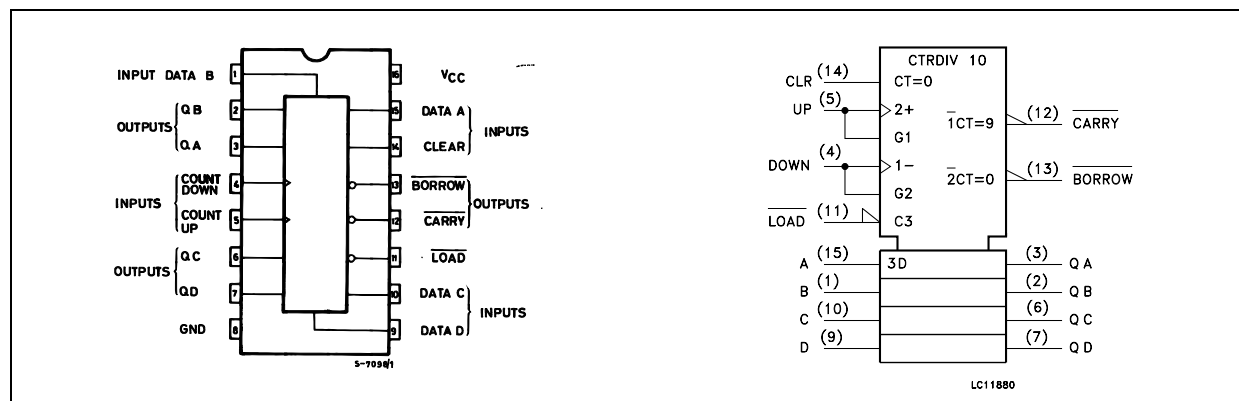
### DESCRIPTION

The M74HC192 is an high speed CMOS SYNCHRONOUS UP/DOWN DECADE COUNTERS fabricated with silicon gate C<sup>2</sup>MOS technology.

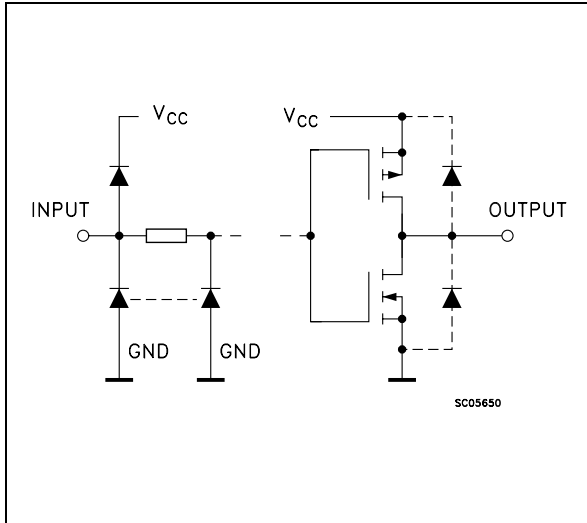
The counter has two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flop are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked. This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D input. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs. In addition

the counter can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to low independently of either COUNT input. Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counters overflows. The counter can be cascaded by connection the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

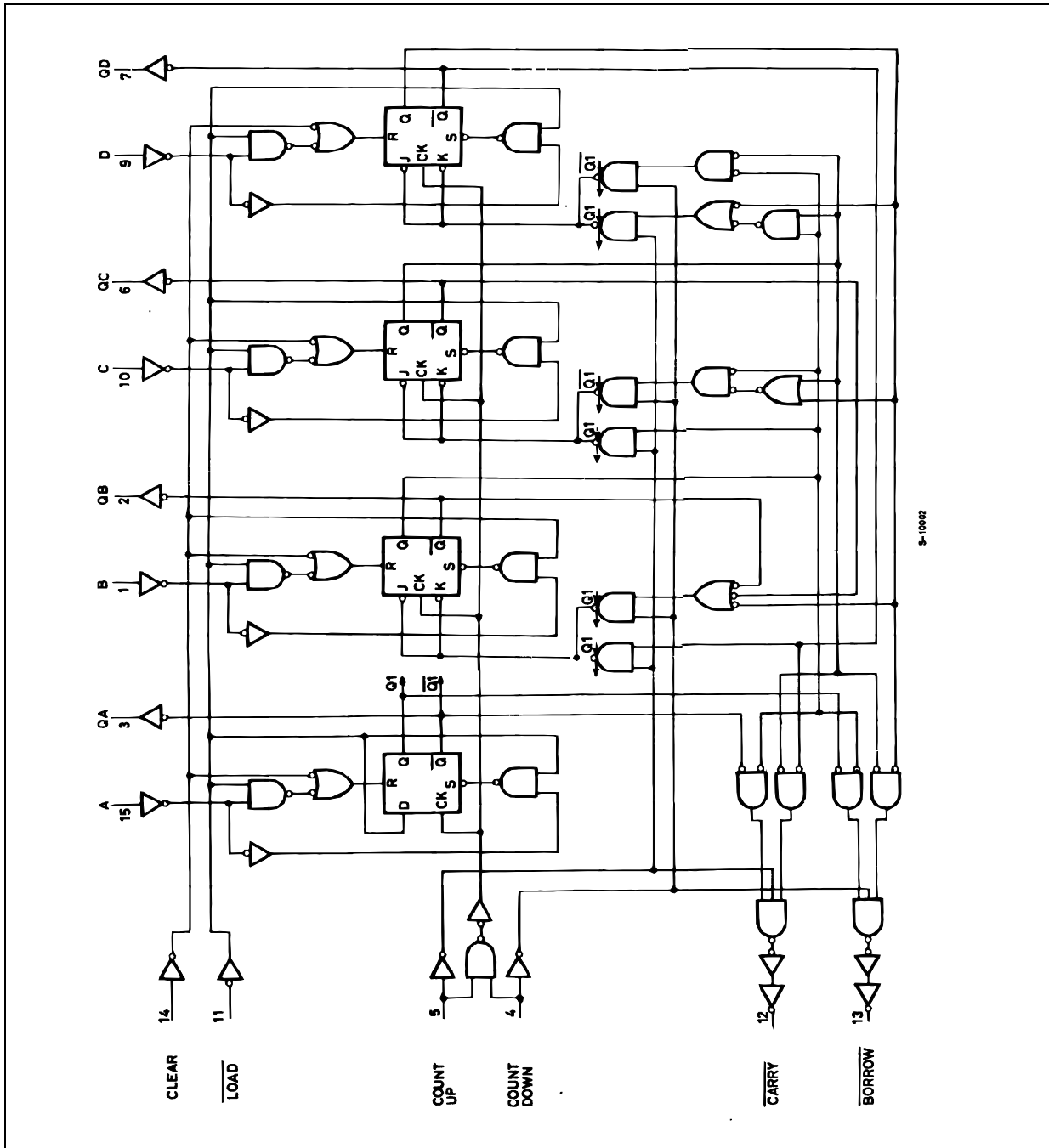
PIN No	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	QA to QD	Flip-Flop Outputs
4	COUNT DOWN	Count Down Clock Input
5	COUNT UP	Count Up Clock Input
11	$\overline{\text{LOAD}}$	Asynchronous Parallel Load Input (Active LOW)
12	$\overline{\text{CARRY}}$	Count Up (Carry) Output (Active LOW)
13	$\overline{\text{BORROW}}$	Count Down (Borrow) Output (Active LOW)
14	CLEAR	Asynchronous Reset Input (Active High)
15, 1, 10, 9	A to D	Data Inputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

COUNT UP	COUNT DOWN	$\overline{\text{LOAD}}$	CLEAR	FUNCTION
	H	H	L	COUNT UP
	H	H	L	NO COUNT
H		H	L	COUNT DOWN
H		H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

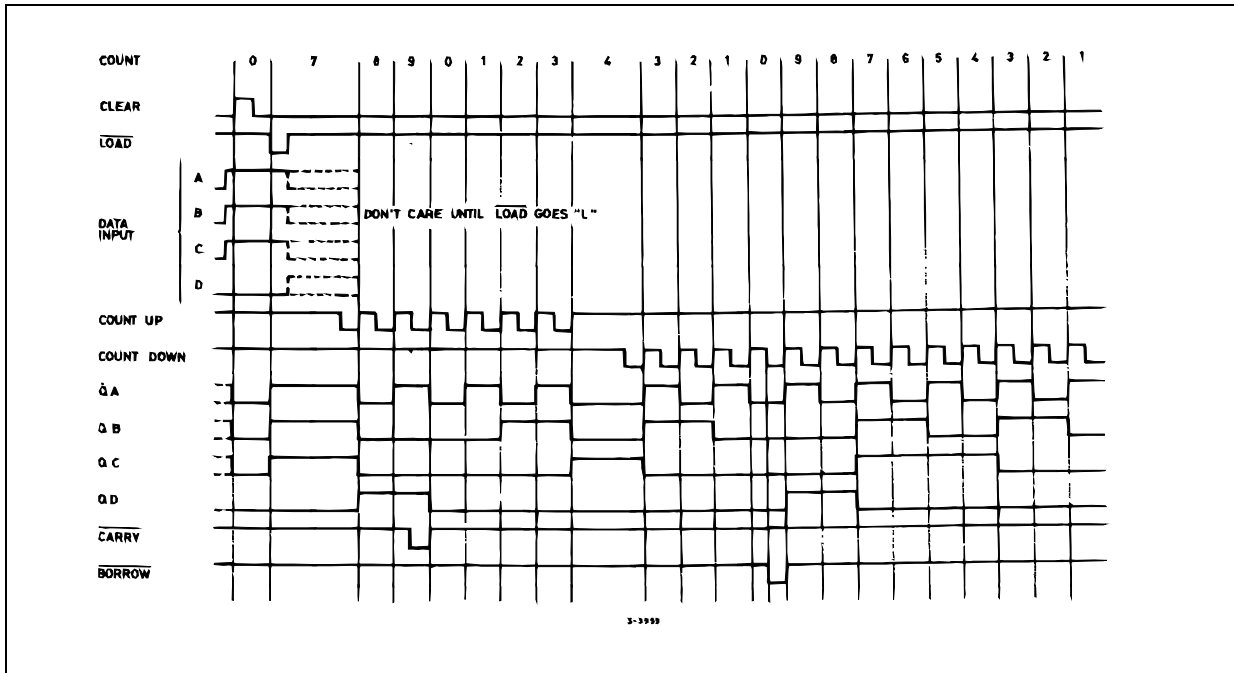
X : Don't Care

LOGIC DIAGRAM



This logic diagram has not been used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$P_D$	Power Dissipation	500(*)	mW
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(\*) 500mW at 65  $^{\circ}C$ ; derate to 300mW by 10mW/ $^{\circ}C$  from 65 $^{\circ}C$  to 85 $^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$	
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V <sub>OH</sub>	High Level Output Voltage	2.0	I <sub>O</sub> =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I <sub>O</sub> =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I <sub>O</sub> =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I <sub>O</sub> =-5.2 mA	5.68	5.8		5.63		5.60		
V <sub>OL</sub>	Low Level Output Voltage	2.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		6.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I <sub>O</sub> =5.2 mA		0.18	0.26		0.33		0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (COUNT UP, DOWN - Q)	2.0			65	190		240		285	ns
		4.5			20	38		48		57	
		6.0			16	32		41		48	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (COUNT UP - CARRY)	2.0			40	130		165		195	ns
		4.5			13	26		33		39	
		6.0			11	22		28		33	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (COUNT DOWN - BORROW)	2.0			40	130		165		195	ns
		4.5			13	26		33		39	
		6.0			11	22		28		33	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (LOAD - Q)	2.0			85	220		275		330	ns
		4.5			25	44		55		66	
		6.0			20	37		47		56	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (LOAD - CARRY)	2.0			110	250		315		375	ns
		4.5			30	50		63		75	
		6.0			25	43		54		64	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (LOAD - BORROW)	2.0			110	250		315		375	ns
		4.5			31	50		63		75	
		6.0			25	43		54		64	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (DATA - Q)	2.0			80	190		240		285	ns
		4.5			25	38		48		57	
		6.0			20	32		41		48	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (DATA - CARRY)	2.0			120	250		315		375	ns
		4.5			34	50		63		75	
		6.0			28	43		54		64	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (DATA - BORROW)	2.0			110	250		315		375	ns
		4.5			30	50		63		75	
		6.0			25	43		54		64	
t <sub>PHL</sub>	Propagation Delay Time (CLEAR - Q)	2.0			100	225		280		340	ns
		4.5			30	45		56		68	
		6.0			25	38		48		58	
t <sub>PLH</sub>	Propagation Delay Time (CLEAR - CARRY)	2.0			120	250		315		375	ns
		4.5			35	50		63		75	
		6.0			29	43		54		64	
t <sub>PHL</sub>	Propagation Delay Time (CLEAR - BORROW)	2.0			120	250		315		375	ns
		4.5			35	50		63		75	
		6.0			29	43		54		64	
f <sub>MAX</sub>	Maximum Clock Frequency	2.0			5	12		4		3.4	MHz
		4.5			25	48		20		17	
		6.0			30	55		24		20	

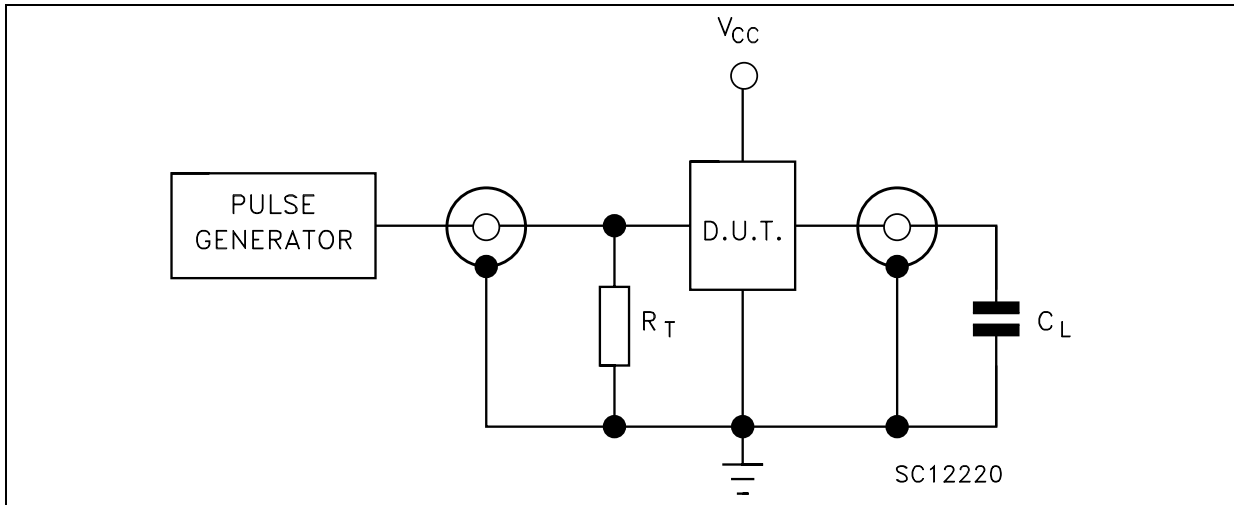
Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>W(H)</sub> t <sub>W(L)</sub>	Minimum Pulse Width (COUNT UP/DOWN)	2.0			34	100		125		150	ns
		4.5			9	20		25		30	
		6.0			7	17		21		26	
t <sub>W(L)</sub>	Minimum Pulse Width (LOAD)	2.0			34	75		95		110	ns
		4.5			9	15		19		22	
		6.0			7	13		16		19	
t <sub>W(H)</sub>	Minimum Pulse Width (CLEAR)	2.0			40	100		125		150	ns
		4.5			12	20		25		30	
		6.0			10	17		21		26	
t <sub>s</sub>	Minimum Set-up Time (DATA -LOAD)	2.0			30	75		95		110	ns
		4.5			9	15		19		22	
		6.0			7	13		16		19	
t <sub>h</sub>	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t <sub>REM</sub>	Minimum Removal Time (LOAD)	2.0			6	50		65		75	ns
		4.5			2	10		13		15	
		6.0			2	9		11		13	
t <sub>REM</sub>	Minimum Removal Time (CLEAR)	2.0			14	50		65		75	ns
		4.5			4	10		13		15	
		6.0			3	9		11		13	

### CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	5.0			5	10		10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	5.0			68						pF

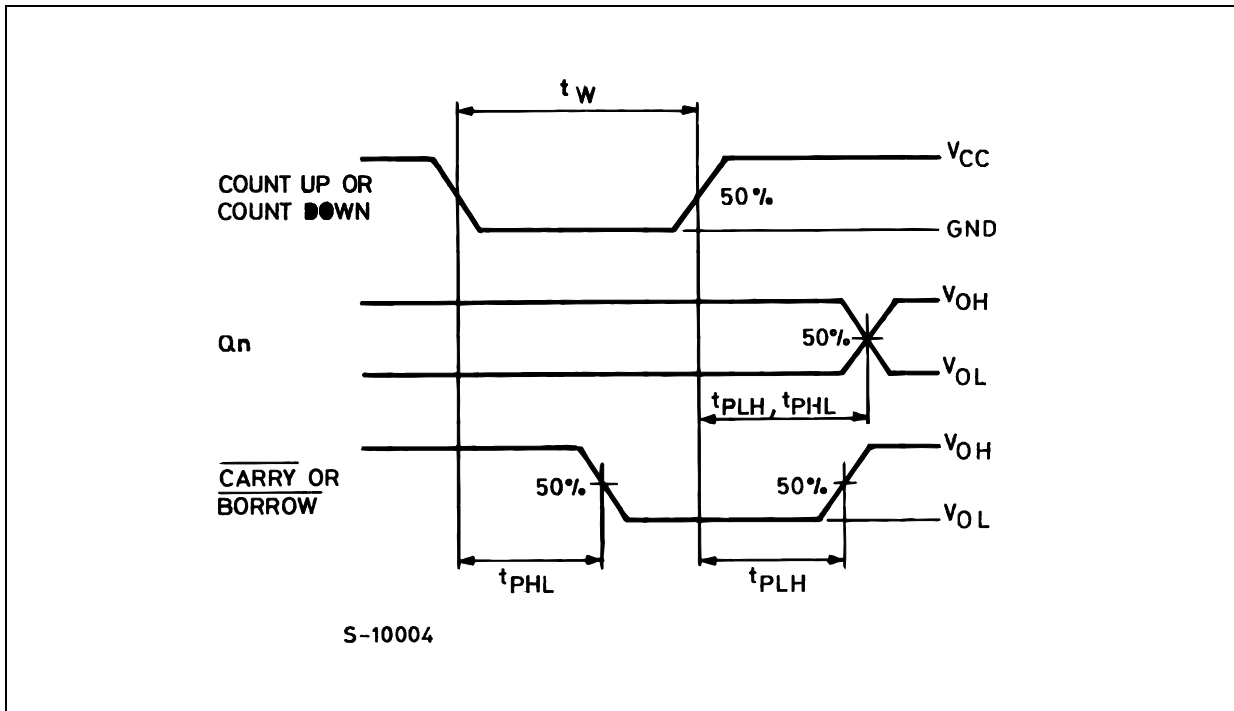
1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

TEST CIRCUIT



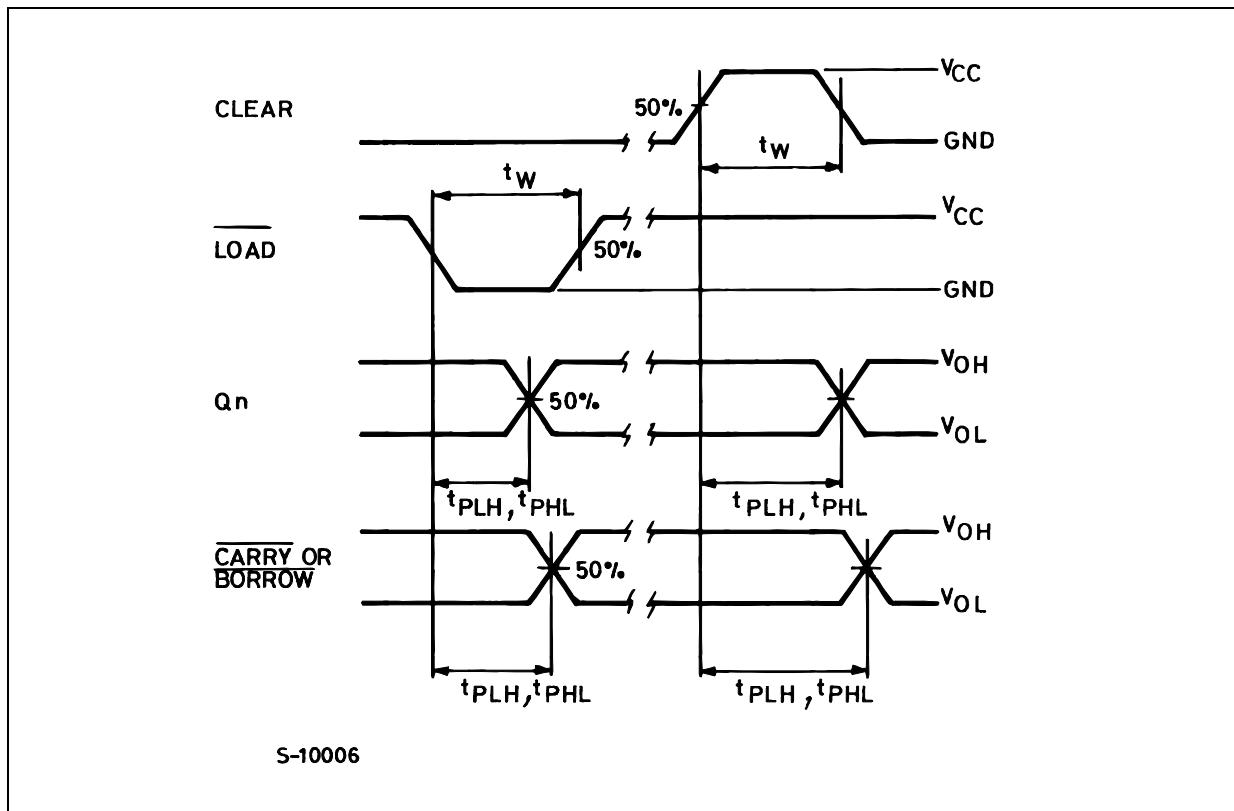
$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**WAVEFORM 1 : PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (COUNT UP AND DOWN)**  
 (f=1MHz; 50% duty cycle)

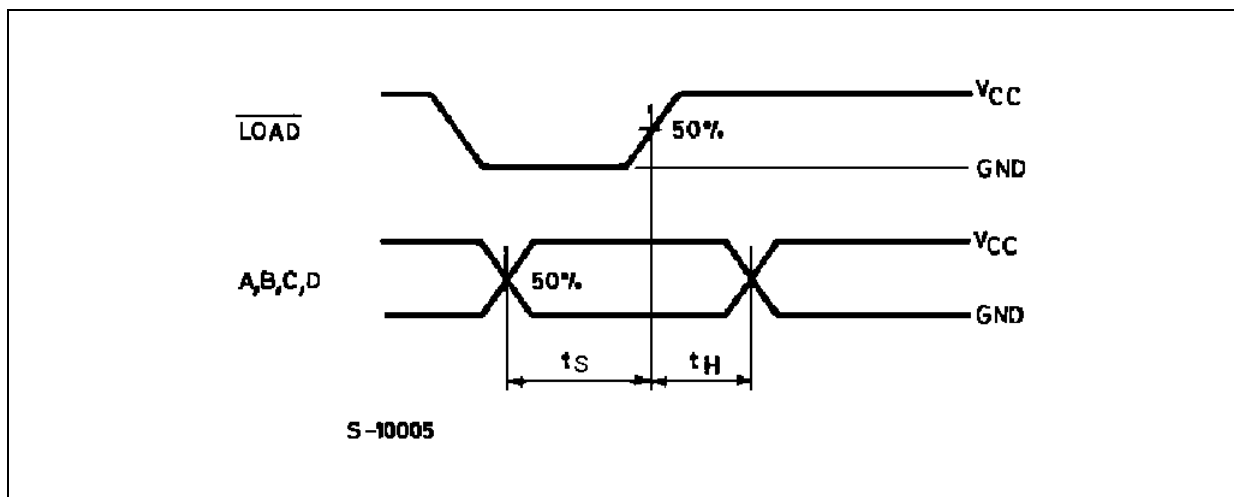




**WAVEFORM 2 : PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (CLEAR,  $\overline{\text{LOAD}}$ )**  
 (f=1MHz; 50% duty cycle)

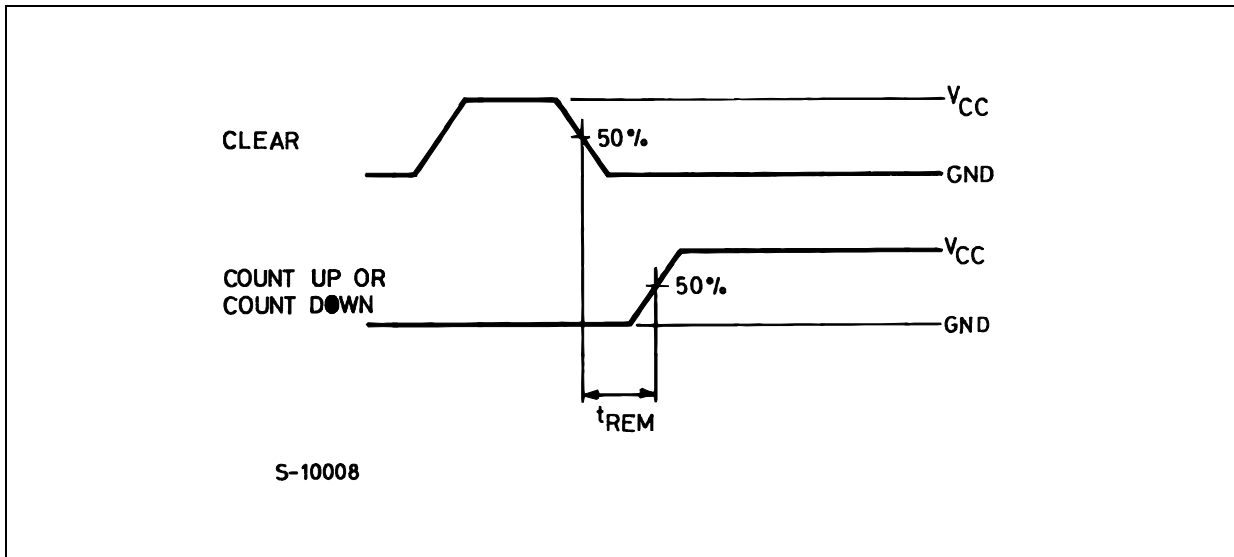


**WAVEFORM 3 : SETUP AND HOLD TIME (A, B, C, D to  $\overline{\text{LOAD}}$ )** (f=1MHz; 50% duty cycle)



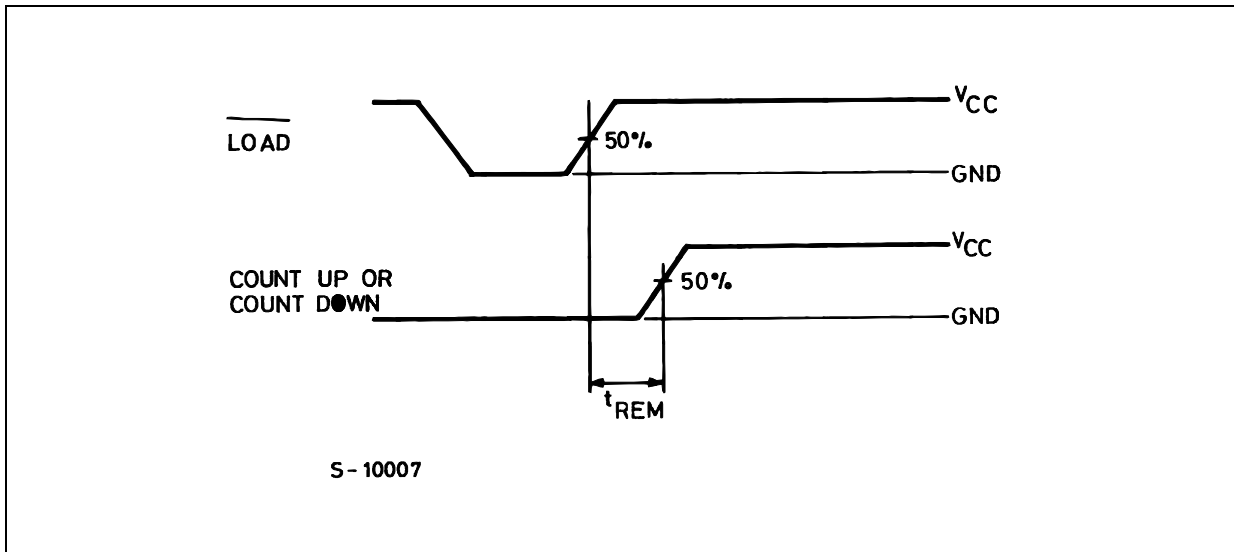
**WAVEFORM 4: MINIMUM REMOVAL TIME (COUNT UP OR DOWN TO CLEAR)**

(f=1MHz; 50% duty cycle)



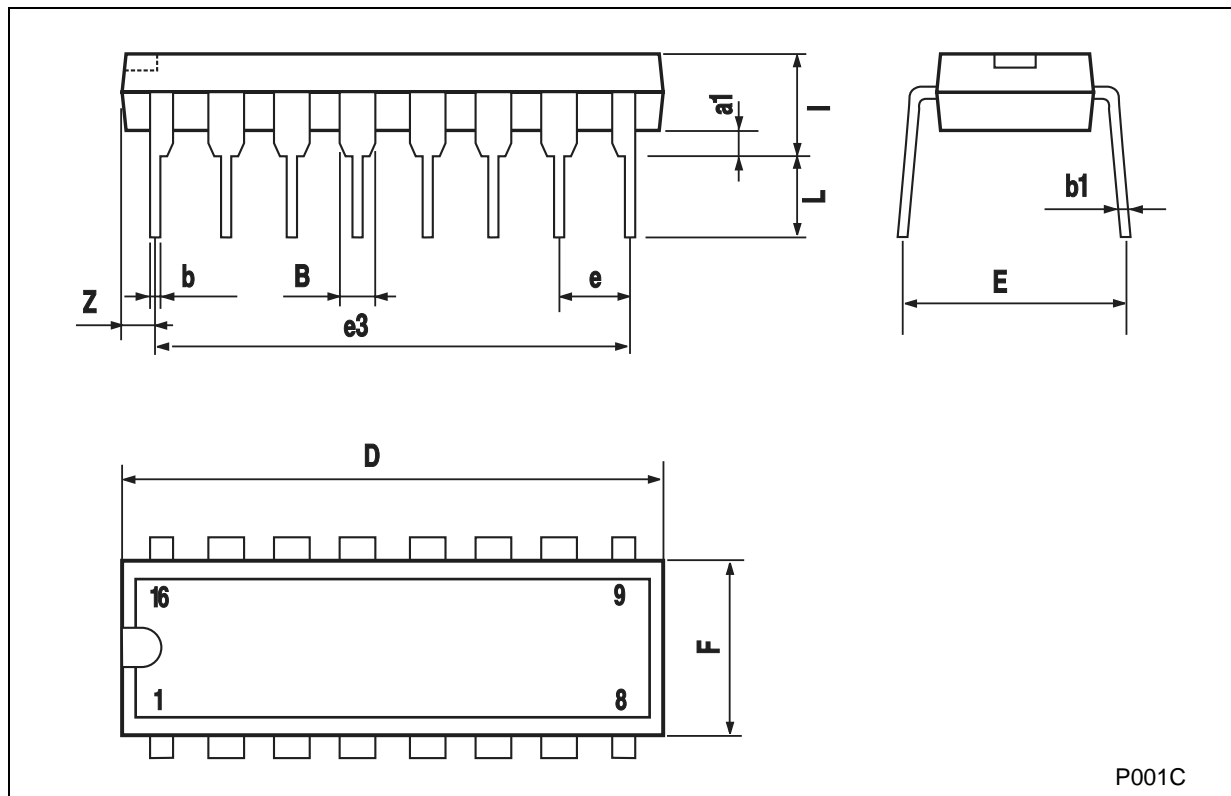
**WAVEFORM 5: MINIMUM REMOVAL TIME (COUNT UP OR DOWN TO  $\overline{\text{LOAD}}$ )**

(f=1MHz; 50% duty cycle)



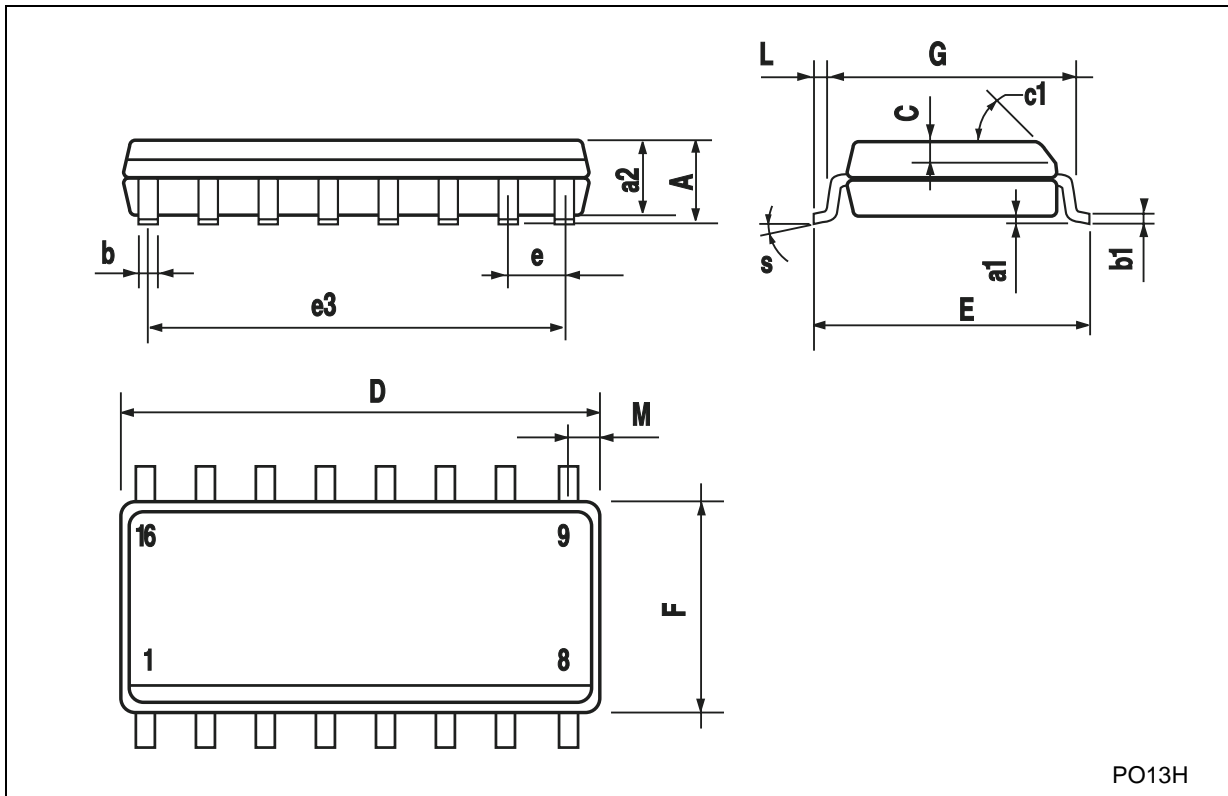
### Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



**SO-16 MECHANICAL DATA**

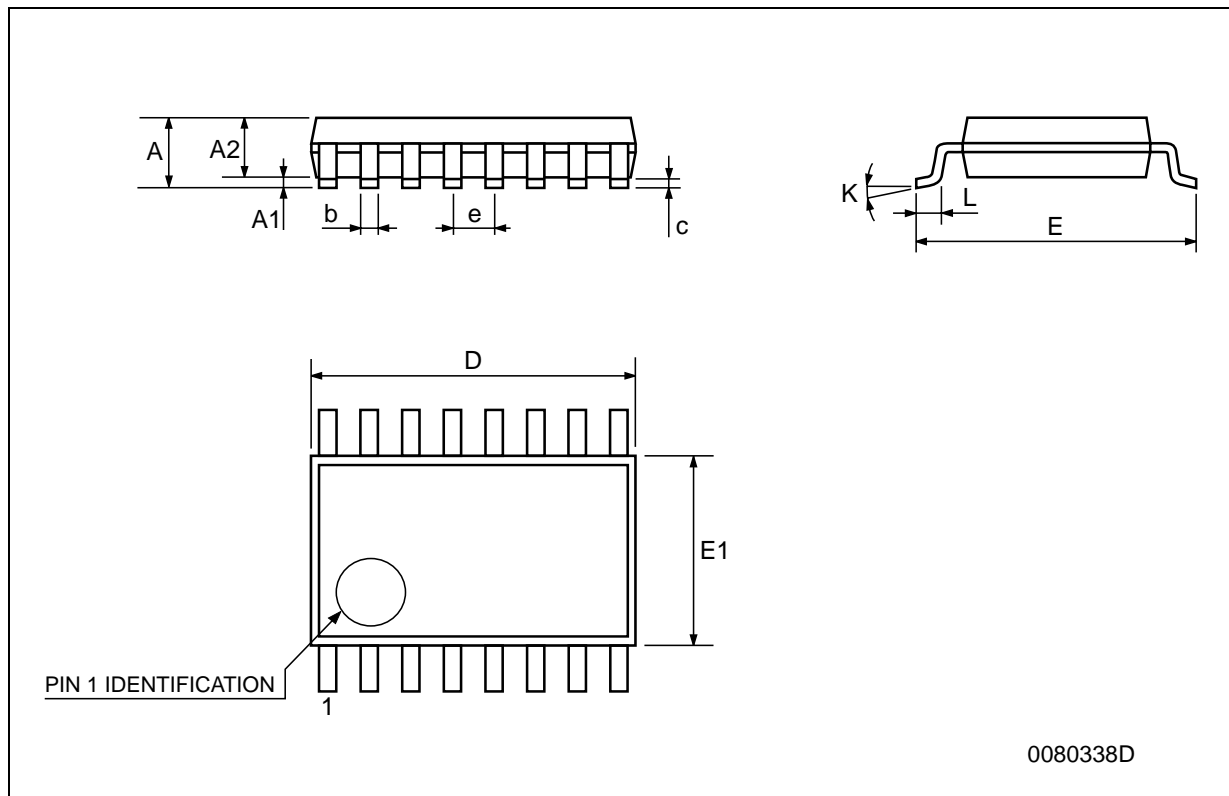
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

## TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>